

**WHAT IS CLAIMED IS:**

- 1 1. A system comprising:
  - 2 a first data processor having an input data port, and an output control port;
  - 3 a memory having a data port to provide output data;
  - 4 a first bit access controller having an input data port coupled to the output data port of the
  - 5 memory, an input control port coupled to the output control port and an output data
  - 6 port coupled to the input data port of the first data processor, the first bit manipulator
  - 7 further including:
    - 8 a plurality of storage locations coupled to the input data port of the first bit
    - 9 manipulator, wherein each storage location stores data having N bit locations
    - 10 including a first bit and a last bit; and
    - 11 a bit shift module having an input port coupled to the plurality of line storage
    - 12 locations, and an output port coupled to the input data port of the first data
    - 13 processor, the shifter to provide at its output shifted bit values that are shifted
    - 14 relative to their storage location within the plurality of line storage locations,
    - 15 wherein the shifted bit values are shifted based on a value received at the
    - 16 input control port.
- 1 2. The system of claim 1 wherein the plurality of storage locations are part of a circular buffer.
- 1 3. The system of claim 2, wherein the circular buffer is used to form a first in first out buffer.
- 1 4. The system of claim 1, wherein the plurality of storage locations are part of a first in first out  
2 buffer.

- 1 5. The system of claim 1 further comprising a memory control portion having a first control  
2 port coupled to a control port of the bit manipulator, and a second control port coupled to a  
3 control port of the memory, wherein the memory control portion requests data from memory  
4 to be stored in the plurality of storage locations.
- 1 6. The system of claim 5 further comprising a watermark storage location to store a value to  
2 indicate the memory control portion is to request data from memory.
- 1 7. The system of claim 1 wherein the first data processor further comprises a general purpose  
2 processor.
- 1 8. The system of claim 7, wherein the general data processor includes a RISC type processor.
- 1 9. The system of claim 8, wherein the RISC type processor includes a MIPS based processor.
- 1 10. The system of claim 9 further comprising a video processor, wherein the video processor is  
2 separate from the first data processor.
- 1 11. The system of claim 9, wherein the video processor includes a video transcoder.
- 1 12. The system of claim 1 further comprising a storage location coupled to the first bit access  
2 controller to store a value indicating an amount of valid data stored in the plurality of storage  
3 locations.

- 1 13. The system of claim 1, wherein the first bit access controller further includes a interrupt  
2 output coupled to an input of the first data processor, where the interrupt output is to be  
3 asserted by the first bit access controller each time a predetermined number of storage  
4 locations of the plurality of storage locations is accessed.
- 1 14. The system of claim 13, wherein the storage location is accessed when it is loaded with data.
- 1 15. The system of claim 13, wherein the storage location is accessed when its data is read.

- 1 16. A method comprising the steps of:  
2 loading a plurality of data words into a storage location based upon a data request by a data  
3 processor;  
4 when in a first mode of operation receiving an indicator from the data processor to  
5 implement a get\_bits request; providing data from the storage location in response  
6 receiving the indicator from the data processor.
- 1 17. The method of claim 16, wherein the step of providing further includes implementing the  
2 get\_bits in hardware.
- 1 18. The method of claim 16, wherein the step of providing further includes user selectively  
2 implementing one of one-filling and zero filling.
- 1 19. The method of claim 16, further comprising the step of:  
2 when in a second mode of operation the indicator from the data processor is to implement a  
3 Huffman decode.

1 20. A method of using a general purpose data processor to access a portion of data bits of a  
 2 plurality of data bits, the method comprising the steps of:  
 3 providing a first request for N data bits to a bit controller, the bit controller being separate  
 4 from the general purpose data processor, where the first bit of the N data bits is not  
 5 aligned on a byte boundary;  
 6 receiving the N data bits from the bit controller;  
 7 determining at the general purpose data processor if M data bits are available from the bit  
 8 controller;  
 9 when the M data bits are available from the controller providing a second request for M data  
 10 bits to the bit controller.

1 21. The method of claim 20 wherein the step of determining includes accessing a register  
 2 associated with the bit controller to determine if M data bits are available.

3 22. The method of claim 20 further comprising the steps of:  
 4 receiving an interrupt indicating an amount of data used by the bit controller;  
 5 modifying an indicator based upon the interrupt, wherein the indicator is used during the  
 6 step of determining to determine if M data bits are available.